(*faculty stamp*)

COURSE DESCRIPTION

1. Course title: DIGITAL SYSTEM DESIGN IN VERILOG HDL	**2. Course code VERILOG**
3. Validity of course description: 2012/2013	
4. Level of studies: BSc programme	
5. Mode of studies: intramural studies	
6. Field of study: ELECTRONIC ENGINEERING	AEII
7. Profile of studies: general-academic	
8. Programme: CEIE	
9. Semester: 6	
10. Faculty teaching the course: Institute of Electronics	
11. Course instructor: Robert Czerwiński	
12. Course classification: specialization	
13. Course status: elective	
14. Language of instruction: English	
15. Pre-requisite qualifications: It is assumed that the student is trained in the basics of digital technology, basics of digital circuit design and the computer programming.	
16. Course objectives: The aim of the course is to familiarize students with the digital systems designing using Verilog hardware description language.	
17. Description of learning outcomes:	

Nr	Learning outcomes description	Method of assessment	Teaching methods	Learning outcomes reference code
1.	Student knows and understands the design methodology of digital electronic systems, as well as the methods and techniques used in the design, student is familiar with hardware description languages and computer tools for design and simulation of circuits and systems	Execution of laboratory exercises	Laboratory	
2.	Student can formulate a simple specification of the electronic systems using hardware description languages	Execution of laboratory exercises	Laboratory	
3.	Student is able to design simple circuits and electronic systems for various applications	Execution of laboratory exercises	Laboratory	
4.	Student is able to think and act in a creative and enterprising way	Execution of laboratory exercises	Laboratory	
5.				
6.				
7.				
8.				

18. Teaching modes and hours

Laboratory

30 h.

19. Syllabus description:

The purpose of the laboratory classes is to familiarize students with the Verilog hardware description language and the designing process using complex programmable logic devices. The first part of the laboratory exercises will be based on writing simple models, synthesizing, implementing and testing. In the second part students are going to implement the project of complex digital circuit.

1. Getting to know the tools for simulation, synthesis and implementation. Writing synthesizable models of combinatorial: translators, multiplexers, decoders, demultiplexers, arithmetic units.

2. Simulation and testing of combinational circuits.
3. Writing synthesizable models of simple sequential circuits: asynchronous flip-flops, synchronization systems with a latch mechanism, edge-triggered systems.
4. Simulation and testing of sequential systems.
5. Writing synthesizable models of complex sequential devices: counters, registers, finite state machines.
6. Modelling complex hierarchical models.
7. Implementation of complex project.

20. Examination: no

21. Primary sources:

Palnitkar S., Verilog HDL. A Guide to Digital Design and Synthesis, Prentice Hall, 2003
Lee W.F., Verilog Coding for Logic Synthesis, John Wiley & Sons Inc., 2003
Lee J.M., Verilog Quickstart: A Practical Guide to Simulation and Synthesis in Verilog, Kluwer Academic Publishers, 2002
Bhasker J., Verilog HDL Synthesis. A practical Primer, Star Galaxy Publishing, 1998
Doulos, The Verilog Golden Reference Guide, Doulos, 1996

22. Secondary sources:

23. Total workload required to achieve learning outcomes

Lp.	Teaching mode :	Contact hours / Student workload hours
1	Lecture	/
2	Classes	/
3	Laboratory	30/15
4	Project	/
5	BA/ MA Seminar	/
6	Other	15/0
	Total number of hours	45/15

24. Total hours: 60

25. Number of ECTS credits: 2

26. Number of ECTS credits allocated for contact hours: 1

27. Number of ECTS credits allocated for in-practice hours (laboratory classes, projects): 2

26. Comments:

Approved:

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(date, Instructor's signature)

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(*date , the Director of the Faculty Unit signature)*