(faculty stamp)

COURSE DESCRIPTION

1. Co	ourse title: Theory of Logic Circuits		2. Course code TLC	
3. Va	lidity of course description: 2017/2018			
4. Le	evel of studies: BA, BSc programme / MA,MSc programme I	u b 1st cycle / 2nd cycle of high	er education	
5. M	ode of studies: intramural studies / extramural studies			
6. Fi	eld of study: Interdisciplinary Studies: Automatic Control and	Robotics, Electronics and	(FACULTY SYMBOL) RAU	
Telecommunications, Computer Science				
7. Pr	ofile of studies: general			
8. Pr	ogramme: all			
9. Se	emester: 1,2			
10. F	aculty teaching the course: Faculty of Automatic Control, E	Electronics and Computer Sci	ence, Institute of Informatics	
11. C	Course instructor: Prof. Krzysztof Cyran, PhD DSc			
12. 0	Course classification: common courses			
13. 0	Course status: compulsory /elective			
14. L	anguage of instruction: English			
15. F	Pre-requisite qualifications: none			
16. C	Course objectives: Theory of Logic Circuits presents to the a	udience a complete course c	overing wide aspects of modern digital sys	tem design
(com	binational, sequential, microprogrammable, programmable),	it's analysis and review. Stud	ents are presented step-by-step course on	general two-value
logic	, numeric systems, algebra and arithmetic of digital devices,	various synthesis and analysi	s methods related to the digital circuits alo	ng with review of digital
devid	ces and their utility.			
17. C	Description of learning outcomes:			
Nr	Learning outcomes description	Method of assessment	Teaching methods	Learning outcomes reference code
1.	Knows various number systems and its arithmetic.	Written test	Lecture and classes	K1A_W4 KIA_W10
2.	Knows algorithms for basic arithmetic operations.	Written test	Lecture and classes	KIA_W10 KIA W3
3.	Knows how to convert number between various numeric systems.	Written test	Lecture and classes	KIA_W10 KIA_W3
4.	Knows Boole algebra, digital circuits structures, knows methodology on digital circuit synthesis and analysis.	Written test	Lecture, classes and laboratory	KIA_W1 K1A_W4 KIA_W10
5.	Is capable to implement combinational and sequential digital circuits in various models and solutions.	Classes: Written test Labs: Evaluation of the circuit implemented, report.	Lecture, classes and laboratory	KIA_W10
6.	Is capable to analyze theoretically and practically various circuits according to its correctness. Is capable to propose corrections and improvements for faulty and non-optimal circuits.	Classes: Written test Labs: Evaluation of the circuit implemented, report.	Lecture, classes and laboratory	KIA_U7 KIA_U12
7.	Performs seamlessly teamwork.	Classes: Written test Labs: Evaluation of the circuit implemented, report.	Lecture, classes and laboratory	KIA_K3
18. T	eaching modes and hours			
Lect	ure / BA /MA Seminar / Class / Project / Laboratory			
Sem 1 - 60 h., Sem 2 - 30 h				

19. Syllabus description:

Semester 1 :

Lecture:

- Numeric systems.
- Converting numbers between different numeric systems.
- Binary forms of numbers and it's representation in digital systems.
- Fixed point arithmetic.
- Information and communication digital vs analogue world.
- Digital devices, circuits and systems.
- Boolean algebra, gates and binary operators.
- System functionally complete.
- Digital systems classification.
- Combinational circuits design.
- Synthesis and analysis of combinational circuits.
- Iterative circuits.
- Sequential digital systems.
- Asynchronous sequential systems design.
- Synchronous sequential systems design.
- Dynamics of sequential systems.
- Microprogrammable circuits design.
- Programmable logic devices.

Classes:

Classroom exercises cover practice of the subjects that are closely related to the lecture, particularly insisting on real problem analysis and solution.

Semester 2:

Laboratory:

Laboratory course covers systems design on digital systems and computer systems. Students are creating and analyzing real digital systems, built of various operators and medium scale integration devices (including sequential-related components and microprogrammable related memory components).

20. Examination: none

21. Primary sources:

U. Stańczyk, K. Cyran, B. Pochopień, Theory of Logic Circuits, vol. I – Fundamental issues, Publishers of the Silesian University of Technology, Gliwice 2007. U. Stańczyk, K. Cyran, B. Pochopień, Theory of Logic Circuits, vol. II – Circuit design and analysis, Publishers of the Silesian University of Technology, Gliwice 2007.

22. Secondary sources:

M. Adamski, A. Barkalov, Architectural and sequential synthesis of digital devices. University of Zielona Góra, 2006. 23. Total workload required to achieve learning outcomes

	Taashing made :	Contract hours / Chudont workland hours
Lp.	Teaching mode :	Contact nours / Student workload nours
1	Lecture	30/45
2	Classes	30/45
3	Laboratory	30/30
4	Project	1
5	BA/ MA Seminar	1
6	Other	1
	Total number of hours	90/120
24. Tota	hours:210	
25. Num	ber of ECTS credits: 7	
26. Num	ber of ECTS credits allocated for contact hours	:: 3
27. Num	ber of ECTS credits allocated for in-practice ho	urs (laboratory classes, projects):2
26. Com	ments:	

Approved:

(date , the Director of the Faculty Unit signature)

(date, Instructor's signature)