(pieczęć wydziału)

SUBJECT INFORMATION

1. Subject name: COMPUTER ARCHITECTURE	**2. Subject code:**
3. Subject information available since academic year: 2018/2019	
4. Form of education: first level study	
5. Form of study: full-time studies	
6. Field of study: COMPUTER SCIENCE; INSTITUTE AEII	
7. Profile of study: academic	
8. Specialty:	
9. Semester: 5, 6	
10. Object providing unit: Institute of Computer Science, RAu2	
11. Subject leader: Zghidi Hafed , PhD	
12. Belonging to a group of subjects: common subjects	
13. Subject status: mandatory	
14. Subject language: english	
15. Intorductory courses and prerequisities: Theory of Computer Science, Micro Informatics.	
16. Subject goal: The lectures are to familiarize students with main concepts related to computer architecture. They present the main directions of development of computer architecture, provide representative examples of computer organization. The main part of the lecture is to present the architecture of modern processors and parallel computers. The purpose of the laboratory is practical and introduce students to various computer architectures, different operating systems and technologies of parallel and distributed programming. Students are familiarized with computers based on Sparc processors, PowerPC, x86, running under control of different operating systems (Windows, Linux, Sun Solaris, OS/400).	

17. Education effects:

Nr	Description of the effect of education	The method of checking education effect	Teaching form	The reference to the effects
W1	Knowledge of the essential elements of construction of processors and computers. Understanding the differences between computers with the Complex Instruction Set Computers (CISC) and Reduced Instruction Set Computers (RISC).	SP	WM, WT	K1A_W05
W2	Understanding the concept and issues of pipelining, jump instructions execution jumps and pipelined implementation of instructions with dependent arguments. Knowledge of the method of branch prediction.	SP	WM, WT	K1A_W08
W3	Knowledge of the of the superscalar architecture concept and VLIW architecture. Knowledge of hardware mechanisms supporting multithread	SP	WM, WT	K1A_W10

	mechanisms. Understanding the general concept of CUDA architecture..			
W4	Knowledge of parallel computers classification, Flynn classification. Knowledge the basic architecture of parallel computers: vector and array computers, multiprocessor systems and clusters.	SP	WM, WT	K1A_W10
W5	Knowledge of main the characteristics of multiprocessor systems with shared memory, distributed memory and non-uniform memory access systems.	SP	WM, WT	K1A_W10, K1A_W16
W6	Knowledge of the organization of high-performance clusters and high-reliability clusters.	SP	WM, WT	K1A_W10, K1A_W16
U1	Ability to assess the effect of CPU performance (number of cores, cache size) on the effectiveness of the programs in the context of the size of the processed data.	SP, CL, PS	WT, L	K1A_U10, K1A_U14
U2	Ablity to assess the effect of a multiprocessor system or cluster system for performance of implemented algorithm according to the size of the processed data.	SP, CL, PS	WT, L	K1A_U23
U3	Knowing how to use parallel programming environment such as PVM, JavaSpaces to implement parallel algorithms.	SP, CL, PS	L	K1A_U18
K1	Competence in choosing appropriate architecture and performance of a computer system according to the needs of the planned IT system	CL, PS	WT, L	K1A_K03

18. Education forms a number of hours
Lectures : 30 Laboratory: 30

19. The content of education:

Lectures

The history of the development of computer architectures: the first computers, the impact of electronic technology in computer architecture, subsequent generations of computers. Complex Instruction Set Computers (CISC). Reduced Instruction Set Computers (RISC): bases, implementation of RISC I computer. Pipelining, the problem of implementing jump instructions (jumps, delayed, branch prediction) and the problem of dependent data (changing the instruction order). Superscalar architecture and VLIW architecture. The specificity of the problems of pipelined instruction execution with dependent arguments in superscalar architecture. Renaming of registers. Examples of the superscalar processor architectures: UltraSPARC, Motorola, PowerPC, POWER. Hardware support for multithreading: fine-grained multithreading, coarse and concurrent.
Architecture of parallel computers. Classification of parallel systems - forms of parallelism: instruction-level parallelism and parallelism of processors, the Flynn classification, other classifications. Vector Computers: scalar and vector instructions - a vector computer concept, a review of vector instructions. Examples of vector computers, the use of vector computers. Array computers: the general approach, the model in the implementation of SIMD commands, interconnect network, examples of array computer. SIMD model in modern superscalar processors. Graphics Cards and the CUDA architecture. Multithreaded - SIMT model. multiprocessor systems

: Systems with shared memory: cache coherence, MESI protocol different ways system elements connections - a common bus, multiple bus systems, cross-bar, multiport memory, multi-stage switch, non-blocking Clos network. NUMA architecture systems. Examples of commercial shared memory systems. Distributed memory systems: MPP model, connecting networks, the role of the processor in communication and transmission - the first and second generation, the development of systems with distributed memory systems: example of Intel and IBM processors. MPP systems on the TOP500 list. Clusters: definition and properties. Network connecting clusters: Topology "fat tree" network Infiniband. Beowulf Clusters. High-performance clusters. Physical construction of the clusters: rack and blade systems. Examples of clusters. MPP clusters in Top 500 list. Clusters with high reliability. Factors constituting high reliability of the clusters: Redundant nodes, access to shared resources, mechanisms for controlling the operation of nodes. Heterogeneous computer systems - conventional CPU processors support by GPUs.

Laboratory

A detailed set of laboratory exercises:
AS/400 – Communication and data access on the AS/400 system
Sparc - Sparc processor low-level programming
CUDA - parallel programming of graphics processing units (GPUs) in C / C + + with corresponding extensions
PVM - Parallel Programming with dynamic allocation of tasks using messages passing architecture using the parallel virtual machine
Mosix – Use of a cluster of workstations for parallel computing and balance load
JavaSpaces – Parallel programming using shared and distributed memory in Java

20. Exam: yes; written, two parts.

21. Basic literature:

A.S. Tanenbaum, Structured Computer Organization. Helion, 2006
W. Stallings, Organizacja i architektura systemu komputerowego. Projektowanie systemu a jego wydajność. WNT, W-wa, 2004.

22. Literatura uzupełniająca:

L. Null, J. Lobur, Struktura organizacyjna i architektura systemów komputerowych, Helion, 2004
J. Kitowski, Współczesne systemy komputerowe, CCNS, Kraków, 2000.
S. Kozielski, Z. Szczerbiński, Komputery równoległe, architektura, elementy programowania. WNT, Warszawa, 1994

23. Student workload required to achieve the effects of education

Lp.	Type of course	Number of contact hours / students workload
1	Lecture	30/20
2	Exercise	0/0
3	Laboratory	30/25
4	Project	0/0
5	Seminar	0/0
6	Other	10/15
	Total hours	70/60

24. The sum of all hours: 130

25. ECTS:[1] points 5
26. Number of ECTS credits gained in the classroom with the direct participation of an academic teacher: 2
27. Number of ECTS credits gained in the class of practical (laboratories, projects): 2
26. Comments:

Approval:

…… ……

(date and signature of leading) *(data and signature of the director of the institute / head of the department / Director of the College of Foreign Languages / manager or inter-unit director)*

[1] 1 punkt ECTS – 25-30 godzin.