## Załącznik Nr 5 do Zarz. Nr 33/11/12

**COURSE DESCRIPTION** 

(pieczęć wydziału)

Z1-PU7 WYDANIE N1 Strona 1 z 3

| 1. 0   | Course title: DIGITAL CIRCUIT  | S DESIGN                       | 2. Course code: D    | CD                   |  |
|--|--|--------------------------------|----------------------|----------------------|--|
| 3. Validity of course description: 2018/2019   |  |                                |                      |                      |  |
| 4. Level of studies: first degree  |  |                                |                      |                      |  |
| 5. M   | lodel of studies: stationary   |                                |                      |                      |  |
| <b>6.</b> Fi   | ield of study: INFORMATICS   |                                |                      |                      |  |
| <b>7.</b> P  | rofile of studies: general academi   | c                              |                      |                      |  |
| <b>8.</b> P  | rogramme: ALL  |                                |                      |                      |  |
| 9. Se  | emester: 3   |                                |                      |                      |  |
| <b>10.</b> I   | F <b>aculty teaching the course:</b> Fac   | ulty of Automatic Control, E   | lectronics and Com   | puter Science,       |  |
| Insti  | tute of Informatics  |                                |                      |                      |  |
| 11. (  | Course instructor: Ph.D. Eng. Kr   | zysztof Tokarz                 |                      |                      |  |
| 12. 0  | Course classification: general   |                                |                      |                      |  |
| 13. 0  | Course status: obligatory  |                                |                      |                      |  |
| 14. I  | Language: English  |                                |                      |                      |  |
| 15. I  | Pre-requisite qualifications: Elec   | ctronics and Measurements, I   | Digital Circuits The | ory, Arithmetic of   |  |
| Digital Systems  |  |                                |                      |                      |  |
| 16. 0  | Course objectives:   |                                |                      |                      |  |
| The object is to present functional properties, dynamic and static digital integrated circuits and the rules |  |                                |                      |                      |  |
| for t  | heir use in construction of digital  | devices. It gives the basic kr | nowledge about func  | ctioning of elements |  |
| of computers and internal modules of microprocessors.  |  |                                |                      |                      |  |
| 17. Description of learning outcomes: <sup>1</sup>   |  |                                |                      |                      |  |
| Nr   | Learning outcomes description  | Method of assessment           | Teaching<br>methods  | Reference code       |  |
| 1  | Student has the general<br>knowledge, including functional<br>properties, dynamic and static<br>digital circuits as well as design<br>and construction rules of digital<br>devices in different<br>technologies. | Test                           | Lecture, classes     | K1A_W05<br>K1A_W07   |  |
| 2  | Student knows the basic<br>methods, techniques and tools<br>used to solve simple tasks from<br>the scope of digital system<br>design   | Test                           | Lecture, classes     | K1A_W22              |  |

<sup>&</sup>lt;sup>1</sup> należy wskazać ok. 5 – 8 efektów kształcenia

| 3     | Student has the skill to design  | Test                  | Lecture, classes                        | K1A_U28                |  |  |
|-------|--|-----------------------|---|------------------------|--|--|
|       | simple digital circuits.   |                       |   |                        |  |  |
|       |  |                       |   |                        |  |  |
|       |  |                       |   |                        |  |  |
|       |  |                       |   |                        |  |  |
|       |  |                       |   |                        |  |  |
| 18.   | Teaching modes and hours   |                       |   |                        |  |  |
| Lec   | ture / BA /MA Seminar / Class / P  | roject / Laborato     | ry:                                     |                        |  |  |
| 30/   | 0/0/15/0/0 (sem.3)   |                       |   |                        |  |  |
| 19 \$ | yllabus description:   |                       |   |                        |  |  |
| Lect  | ure  |                       |   |                        |  |  |
| Intro | oduction, classification, purpose and  | area of application   | ns of digital devices.                  |                        |  |  |
| Basi  | c techniques for the implementation  | of integrated circu   | iits (TTL, CMOS).                       |                        |  |  |
| Stat  | ic, dynamic and functional paramete  | rs of integrated cire | cuits.                                  |                        |  |  |
| Con   | nparison of different implementation   | techniques. Input,    | control, processing blocks, output c    | levices.               |  |  |
| Inte  | grated functional modules: 3-state b   | uffers, multiplexers  | s, encoders, decoders, code converte    | rs, priority coders,   |  |  |
| cou   | nters, registers, arithmetic systems, p  | oarallel transfer sys | tems, parity bit generators, time circ  | uits, generators,      |  |  |
| sem   | iconductor memories, programmable  | e PLD logic structu   | ares, displays, AD and DA converter     | rs.                    |  |  |
| Bus   | es. Parallel asynchronous and synchronous and synchr | ronous registers and  | d counters.                             |                        |  |  |
| RAI   | M memories - static SRAM and dyna  | amic DRAM (asyn       | chronous and synchronous). Ways t       | o refresh the contents |  |  |
| of D  | RAM memory. Building blocks of I   | RAM with a given      | organization.                           |                        |  |  |
| ROI   | M memories, PROM, EPROM, E2P   | ROM, FLASH. Co        | nstruction of fixed memory blocks w     | with a given           |  |  |
| orga  | nization.  |                       |   |                        |  |  |
| Prog  | grammable logical PLD structures. P  | rogramming of per     | manent memories and PLD systems         | š.                     |  |  |
| Digi  | tal signal transmission. Transmissio   | n lines, asymmetrie   | cal and symmetrical, line transmitter   | rs and receivers.      |  |  |
| Inpu  | it systems: buttons, keyboards. Outp   | ut systems, seven-s   | segment displays, LCD, numeric, al      | phanumeric, matrix,    |  |  |
| LEI   | ) matrix displays.   |                       |   |                        |  |  |
| Dist  | urbances in digital circuits (external   | , internal: crosstalk | , reflections) and ways of limiting the | neir impact            |  |  |
| (shi  | elding, blocking, wave fitting).   |                       |   |                        |  |  |
| Dan   | hage to digital circuits and their mod   | els. Testing digital  | circuits. Methods of test generation    |                        |  |  |
| Lau   | Launching of digital circuits. Logic analyzers, signature analyzers.   |                       |   |                        |  |  |
| Prin  | ciples of designing digital devices. I   | Power and assembly    | y rules of electronic digital devices.  |                        |  |  |
| Clas  | sses   |                       |   |                        |  |  |
| Dur   | ing the classes the examples of desig  | gning typical syster  | ns are presented with the necessary     | calculations related   |  |  |
| to, f | or example, the selection of resistor  | values for OC type    | outputs or counting the current lim     | it of outputs.         |  |  |
| 20.   | Exam: no   |                       |   |                        |  |  |
| 21.   | Primary sources:   |                       |   |                        |  |  |
|       | 1. M. Łakomy, J. Zabrodzki "C  | Cyfrowe układy so     | calone" PWN, 1983 r.                    |                        |  |  |

M. Łakomy, J. Zabrodzki "Układy scalone CMOS" PWN, 1995 r.

## 22. Secondary sources:

1. M. Łakomy, J. Zabrodzki "Liniowe układy scalone w technice cyfrowej" PWN, 1987 r.

| 2. J. Pieńkowski, J. Turczyński "Układy scalone TTL w systemach cyfrowych" WKiŁ, 1980r |               |  |  |  |  |  |
|--|---------------|--|--|--|--|--|
| 23. Total workload required to achieve learning outcomes                               |               |  |  |  |  |  |
| Lp.  | Teaching mode | Contact hours / Student workload hours |  |  |  |  |
| 1  | Lecture       | 30/20                                  |  |  |  |  |
| 2  | Classes       | 15/15                                  |  |  |  |  |
| 3  | Laboratory    | /                                      |  |  |  |  |

**24. Total hours:** 90

Total number of hours

**25. Numbers of ECTS:** 3

Project

Seminar

Other

**26. Number of ECTS credits allocated for contact hours:** 2

27. Number of ECTS credits allocated for in-practice hours (laboratory classes, projects): none

26. Comments:

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Approved:

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5/5

50/40

..... (date, Instructor's signature)

..... (date, the Director of the Faculty Unit signature)